ABSTRACT OF THE DISCLOSURE

A semiconductor memory device and method for making the same, where a memory cell and high voltage MOS transistor are formed on the same substrate. An insulating layer is formed having a first portion that insulates the control and floating gates of the memory cell from each other, and a second portion that insulates the poly gate from the substrate in the MOS transistor. The insulating layer is formed so that its first portion has a smaller thickness than that of its second portion.